IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ĺ'n	re	an	plic:	ation	of:

Hung T. Nguyen

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For:

EFFICIENT INSTRUCTION PREFETCH MECHANISM EMPLOYING SELECTIVE VALIDITY OF CACHED INSTRUCTIONS FOR DIGITAL

SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

Group No.:

Examiner: Tonia L. Meonske

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Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

To 0110CU 14 2007

Kacen Vestz

Sir:

Karen Viert (Signature of the person signing the cerpificate)

ASSERTION OF SMALL ENTITY STATUS (37 CFR § 1.27(c)(1)

Applicant hereby states that applicant is a small entity and that status as a small entity is asserted for this

___ application

X patent.

Respectfully submitted,

Registration No. 33,182

Date: January 16, 2007

P.O. Box 832570 Richardson, Texas 75083 (972) 480-8800